IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Praveen Parvathala	Examiner: John J. Tabone
Serial No.:	09/917,661	Group Art Unit: 2133
Filed:	July 31, 2001	Docket No.: 80107.051US1
Title:	FUNCTIONAL RANDOM INSTRUCTION TESTING (FRIT) METHOD FOR COMPLEX DEVICES SUCH AS MICROPROCESSORS	

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.116

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant has reviewed the Final Office Action mailed on December 16, 2004. Please amend the above-identified patent application as follows.